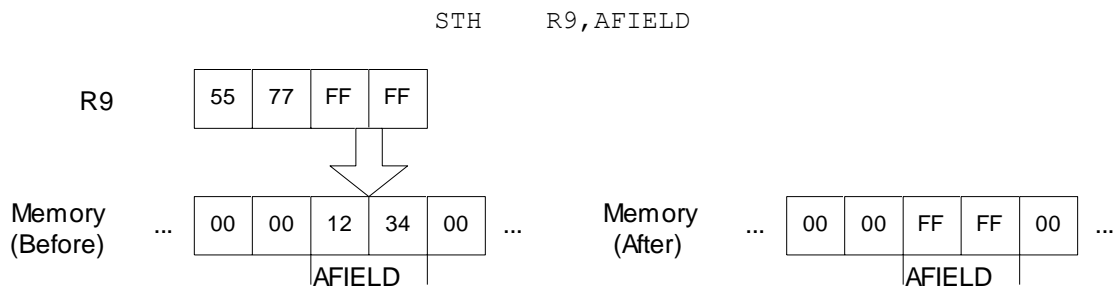


The **STH** instruction has two operands: the first operand is a general purpose register, and the second operand is a halfword storage area in memory. The effect of the instruction is to copy the contents of bits 16-31 of the Operand 1 register (the rightmost two bytes) into the halfword specified by Operand 2. The condition code is unaffected by this instruction. Consider the following example.



The rightmost two bytes of register 9 are copied to the halfword AFIELD, destroying the previous contents. The register value is unchanged by this operation.

Since **STH** is an RX instruction, an index register may be coded as part of operand 2 (see Explicit Addressing).

Examples

Some Unrelated Store Halfwords

R4 = X'00000000'
 R5 = X'12345678'
 R6 = X'00000004'

AFIELD	DC	H'4'	AFIELD = X'0004'
BFIELD	DC	H'25'	BFIELD = X'0019'
CFIELD	DC	H'0'	CFIELD = X'0000'

STH	R4,AFIELD	AFIELD = X'0000'
STH	R4,BFIELD	BFIELD = X'0000'
STH	R4,CFIELD	CFIELD = X'0000'
STH	R5,AFIELD	AFIELD = X'5678'

```
STH R6,BFIELD BFIELD = X'0004'
```

CONSIDER THE NEXT TWO CONSECUTIVELY EXECUTED INSTRUCTIONS

```
LH R8,AFIELD R8 = X'00000004'
```

```
STH R5,AFIELD(R8) BFIELD = X'5678'
```