The Exclusive Or Register instruction performs a logical bit by bit “exclusive or” between two registers. Operand 1, the target, is a register and Operand 2, the source, also specifies a register. The fullword in Operand 1 is exclusive or-ed internally with the fullword in Operand 2, and the result is placed in Operand 1. The table below shows the results of “exclusive or-ing” two bits together.

<table>
<thead>
<tr>
<th>Bit 1</th>
<th>Bit 2</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

This instruction sets the condition code as follows:

0 if all target bits are set to 0. Test this condition with \texttt{BZ} or \texttt{BNZ}.
1 if any target bit is set to 1. Test this condition with \texttt{BM} or \texttt{BNM}.

Examples

Some Unrelated Exclusive Or Registers

\begin{verbatim}
R4 = X'FFFFFFFF'    ALL 1's
R5 = X'00000000'    ALL 0's
R6 = X'0000148C'    00000000000000000001010010001100
R7 = X'000014AB'    00000000000000000001010010101011
XR R4,R4  R4 = X'00000000' Condition Code = 0
XR R4,R5  R4 = X'FFFFFFFF' Condition Code = 1
XR R4,R6  R4 = X'FFFFFFEB73' Condition Code = 1
XR R4,R7  R4 = X'FFFFFFE54' Condition Code = 1
XR R5,R6  R5 = X'0000148C' Condition Code = 1
XR R5,R7  R5 = X'000014AB' Condition Code = 1
XR R6,R7  R6 = X'00000027' Condition Code = 1
XR R7,R7  R7 = X'00000000' Condition Code = 0
\end{verbatim}